

CLAIMS

- 1 1. A tester for testing a plurality of chips, comprising:
- 2 a source of test patterns to stimulate the plurality of chips simultaneously;
- 3 golden output signal; and
- 4 a circuit for simultaneously using outputs of the plurality of chips and said
- 5 golden output signal to determine which chips pass and which chips fail,
- 6 wherein said circuit is located local to said chips.
- 1 2. The tester as recited in claim 1, further comprising:
- 2 a test control device, wherein said test control device controls test patterns
- 3 for testing said plurality of chips in parallel;
- 4 a checking circuit for comparing output signal of said plurality of chips
- 5 with each other in response to said test patterns; and
- 6 wherein said golden output signal is used to replace defective output signal
- 7 from a failing chip.
- 1 3. The tester as recited in claim 2, wherein said test control device controls a test
- 2 engine.

1 4. The tester as recited in claim 3, wherein said test engine comprises a BIST engine.

1 5. The tester as recited in claim 2, wherein said test control device controls a
2 memory with stored patterns.

1 6. The tester as recited in claim 2, wherein said test control device further comprises
2 a switch for turning off signal from a chip and replacing that signal with said
3 golden output signal.

1 7. The tester as recited in claim 6, wherein said switch comprises a MUX.

1 8. The tester as recited in claim 2, further comprising a power supply for providing a
2 power supply voltage, wherein said test control device controls said power supply
3 voltage to provide stress conditions to chips under test.

1 9. The tester as recited in claim 2, further comprising a temperature control for
2 controlling temperature of the plurality of chips, wherein said test control device
3 controls said temperature to provide stress conditions to chips under test.

1 10. The tester as recited in claim 2, wherein said checking circuit compares each chip
2 with all other connected chips.

1 11. The tester as recited in claim 2, wherein said checking circuit comprises an
2 XNOR.

1 12. The tester as recited in claim 11, wherein said XNOR is at least n-way, where n is
2 the number of chips that can be tested.

- 1 13. The tester as recited in claim 12, wherein said XNOR is at least $n+1$ -way, wherein
2 data from a golden chip is always included in data arriving at said XNOR.
- 1 14. The tester as recited in claim 2, wherein said golden output signal is provided by a
2 golden chip.
- 1 15. The tester as recited in claim 14, further comprising a MUX to isolate a chip and
2 to route signal from said golden chip to replace signal from said isolated chip.
- 1 16. The tester as recited in claim 2, further comprising a visible indicator showing
2 passing chips or failing chips.
- 1 17. The tester as recited in claim 16, wherein said visible indicator comprises a light.
- 1 18. The tester as recited in claim 2, further comprising a register for storing passing or
2 failing chip labels.
- 1 19. The tester as recited in claim 2, further comprising sockets for holding the chips,
2 and wherein said sockets, said test control device, said test engine, and said
3 checking circuit are on a single card.
- 1 20. The tester as recited in claim 2, further comprising a memory for storing test
2 results for comparison with golden test result data.
- 1 21. The tester as recited in claim 2, wherein said golden test result data are provided
2 by a golden chip.

1 22. The tester as recited in claim 1, wherein said circuit comprises comparing all chip
2 outputs with corresponding golden test result data and then combines results of all
3 comparisons for each chip into a pass or fail signal from each chip.

4 23. The tester as recited in claim 21, wherein said circuit comprises an array of 2-way
5 XNOR gates and an OR gate for each chip under test.

1 24. The tester as recited in claim 21, wherein said golden output signal is provided by
2 a golden chip.

- 1 25. A device for testing integrated circuit chips comprising a test circuit for
2 connection to a plurality of integrated circuit chips simultaneously, said test
3 circuit for testing said integrated circuit chips during transport.
- 1 26. The device in claim 25, wherein said test circuit compares said integrated circuit
2 chips with each other.
- 1 27. The device in claim 26, wherein said test circuit compares all said integrated
2 circuit chips with all other integrated circuit chip that have not been found to be
3 defective.
- 1 28. The device in claim 25, wherein said test circuit compares all said integrated
2 circuit chips with a golden chip.
- 1 29. The device in claim 25, further comprising a power supply connected to said test
2 circuit, wherein said power supply is for providing a power supply voltage to said
3 test circuit and to the chips.
- 1 30. The device in claim 29, wherein said test circuit controls said power supply
2 voltage to provide stress conditions to chips under test.
- 1 31. The device in claim 25, wherein said test circuit includes a test engine.
- 1 32. The device in claim 31, wherein said test engine comprises a BIST circuit.
- 1 33. The device in claim 31, wherein said test circuit includes a memory.

1 34. The device in claim 25, further comprising an indicator for identifying which of
2 the integrated circuit chips failed said testing.

1 35. The device in claim 34, wherein said indicator comprises a memory.

1 36. The device in claim 34, wherein said indicator comprises a visual indicator.

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1 37. A method of testing a plurality of integrated circuit chips, comprising the steps of:

2 a) providing a source of test patterns to stimulate the plurality of
3 chips simultaneously;

4 b) providing a golden output signal; and

5 c) providing a circuit for simultaneously using outputs of the plurality
6 of chips and said golden output signal to determine which chips
7 pass and which chips fail, wherein said circuit is located local to
8 said chips.

1 38. A method of testing as recited in claim 37, wherein in providing step (a) said
2 source of test patterns comprises a BIST engine or a memory.

1 39. A method of testing as recited in claim 37, further comprising providing a golden
2 chip wherein in providing step (b) said golden output signal comprises output of
3 said golden chip, and wherein in providing step (a) providing said source of test
4 patterns to stimulate said golden chip and the plurality of chips simultaneously.

1 40. A method of testing as recited in claim 37, wherein in providing step (c) said
2 circuit uses said golden output signal to replace output signal from a chip.

1 41. A method of testing as recited in claim 37, wherein in providing step (c) said
2 circuit uses said golden output signal to replace output signal from a defective
3 chip.

1 42. A method of testing as recited in claim 37, wherein in providing step (c) said
2 circuit includes a checking circuit for comparing output signal of said plurality of
3 chips with each other in response to said test patterns.

1 43. A method of testing as recited in claim 37, wherein in providing step (c) said
2 circuit includes a circuit for comparing output signals of said plurality of chips
3 with said golden output signal to determine whether each of said plurality of chips
4 under test passes or fails.

1 44. A method of testing as recited in claim 43, wherein in providing step (b) a golden
2 chip provides said golden output signal.

- 1 45. A method of testing an integrated circuit chip, comprising the steps of:
- 2 a) providing a golden chip;
- 3 b) providing test patterns for testing the chip under test and for testing
- 4 said golden chip; and
- 5 c) comparing an output signal from the chip under test with an output
- 6 signal from said golden chip to determine whether the chip under
- 7 test passes or fails.

- 1 46. The method of testing as recited in claim 45, wherein in providing step (b) said
- 2 test patterns are provided to a plurality of chips under test simultaneously.

1 47. A method for testing integrated circuit chips comprising:

2 a) transporting said integrated circuit chips; and

3 b) testing said integrated circuit chips during said transporting.

1 48. The method in claim 47, further comprising supplying power to a test circuit
2 connected to said integrated circuit chips during said transporting.

1 49. The method in claim 47, further comprising identifying ones of said integrated
2 circuit chips which failed said testing.

1 50. The method in claim 49, wherein said identifying comprises storing results of said
2 testing in a memory.

1 51. The method in claim 49, wherein said identifying comprises displaying a visual
2 indicator of passing or failing chips

1 52. The method in claim 47, wherein said testing includes comparing output signals
2 of said integrated circuit chips with each other.

1 53. The method in claim 47, wherein said testing includes comparing output signals
2 of one integrated circuit chip with output signals of all other integrated circuit
3 chips that have not been identified as defective.

1 54. The method in claim 47, wherein said testing includes comparing output signals
2 of said integrated circuit chips with a golden chip.

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